WHAT IS CLAIMED IS:

1. A multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access the same data area of said common memory, wherein:

said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;

each processor is provided with a storage unit equivalent to the common memory and with an access controller; and

the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts data written to said common memory and data read from said common memory and stores this data in the storage unit within its own processor.

2. The system according to claim 1, wherein identical addresses are allocated to address spaces of the storage unit of each processor and of the common memory, and the access controller of a processor that does not have access privilege writes data on the common bus to a storage area of a storage unit designated by an address on the common bus.

3. The system according to claim 1, wherein when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit, determines whether another processor is busy and, if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory.

4. The system according to claim 1, wherein if, when read-out of data from a prescribed data area in said common memory is commanded by a host apparatus, said data area in said storage unit is valid, then the access controller of a processor that has access privilege reads data from this data area and inputs the data to the host apparatus.

5. The system according to claim 2, wherein when writing of data to a prescribed data area in said

common memory is commanded by the host apparatus, the access controller of a processor that has access privilege writes data to a data area of said storage unit and sends this data as well as an address corresponding to this data area to the common bus.

6. A multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access the same data area of said common memory, wherein:

said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;

each processor is provided with a storage unit equivalent to said control information area and with an access controller; and

the access controller of a processor that does not have access privilege monitors control information and addresses that flow on the common bus, accepts this control information and stores it in the storage unit within its own processor.

7. The system according to claim 6, wherein identical addresses are allocated to the storage unit of each processor and to a control information area of the common memory, and the access controller of a processor that does not have access privilege accepts the control information on the common bus and writes it to a storage area of a storage unit designated by an address on the common bus.

8. The system according to claim 6, wherein when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit, determines whether another processor is busy and, if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory.

9. A multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access the same data area of said common memory, wherein:

said common memory is provided with a number of

data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;

each processor is provided with a storage unit equivalent to said data area and with an access controller; and

the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts this data and stores it in the storage unit within its own processor.